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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

GERGISO, TECHANE

ART UNIT PAPER NUMBER

2137

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/815,484	Applicant(s) CANDELORE ET AL.	
	Examiner Techane J. Gergiso <i>T.G.</i>	Art Unit 2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-23 have been examined.
2. Claims 1-23 are rejected.

Specification

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

100 (page 6: line 20; page 9: line 12); 115 (page 8: line 3); 118 (page 8: line 30); 300 (page 11: line 12); 310 (page 11: line 12); 320 (page 11: line 12); 410 and 430 (page 16: lines 12-14).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 11-13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ansari et al. (US Pub No.: 2004/0221302) in view of Kisliakov et al. (US Pat. No.: 6,289,455).

As per claim 1:

Ansari et al. disclose an apparatus adapted to a digital device, comprising: core logic;
a first conditional access (CA) logic block connected to the core logic, the first CA logic block using a first CA function associated with a first CA provider (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62) ; and
a second CA logic block connected to the core logic, the second CA logic block using a second CA function associated with a second CA provider (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62),
wherein a connection between the first CA logic block is disabled when descrambling of the incoming scrambled content is to be conducted according to the second CA function (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

Ansari et al. do not explicitly teach a core logic. Kisliakov, in an analogous art, however teach core logic (Figure 10: 1044). Therefore, it would have been obvious to a

person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Ansari et al. to include a core logic. This modification would have been obvious because a person having ordinary skill in the art would have been motivated by the desire to allow easy implementation of access control for a smart card systems in relation to certain applications executing on the system suggested by Kisliakov in (Page 2: 0011).

As per claim 2:

Ansari et al. disclose CableCARD coupled to a set-top box (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

As per claim 11:

Ansari et al. disclose an apparatus adapted to a digital device, comprising:

a plurality of conditional access logic blocks coupled to the core logic and including a first conditional access logic block and a second conditional access logic block, the first conditional access logic block using a first conditional access (CA) function associated with a first CA provider and the second conditional access logic block using a second CA function associated with a second CA provider (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62);

wherein enabling only the first conditional access logic block of the plurality of conditional access logic blocks when the incoming scrambled content is

scrambled according to the first CA function (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

Ansari et al. do not explicitly teach a core logic. Kisliakov, in an analogous art, however teach core logic (Figure 10: 1044). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Ansari et al. to include a core logic. This modification would have been obvious because a person having ordinary skill in the art would have been motivated by the desire to allows easy implementation of access control for a smart card systems in relation to certain applications executing on the system suggested by Kisliakov in (Page 2: 0011).

As per claim 12:

Ansari et al. disclose an apparatus, wherein the core logic further comprises a descrambler shared by the plurality of conditional access logic blocks to descramble the incoming data (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

As per claim 13:

Ansari et al. disclose an apparatus, wherein each of the plurality of conditional access logic blocks further comprises a descrambler to descramble the incoming data (Page 2: 0021).

As per claim 20:

Ansari et al. disclose an apparatus adapted for coupling to internal circuitry of a digital device and for descrambling incoming scrambled content, comprising:

a programmable logic device including a plurality of programmable gates programmed to operate in accordance with a conditional access (CA) function associated with a first CA provider to descramble the incoming scrambled content (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

Ansari et al. do not explicitly teach a core logic. Kisliakov, in an analogous art, however teach core logic (Figure 10: 1044). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Ansari et al. to include a core logic. This modification would have been obvious because a person having ordinary skill in the art would have been motivated by the desire to allows easy implementation of access control for a smart card systems in relation to certain applications executing on the system suggested by Kisliakov in (Page 2: 0011).

6. Claims 3-10, 14-19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ansari et al. (US Pub No.: 2004/0221302) in view of Kisliakov et al. (US Pat. No.: 6,289,455) in further view of Kocher et al. (US Pat. No.: 6, 289, 455).

As per claim 3:

Kisliakov teaches an apparatus, wherein the core logic comprising:

a processor core (Figure 10: 1044);
a non-volatile memory accessible by the processor core, the non-volatile memory to contain information in a scrambled format, the information being recovered using the key contained in the secure non-volatile memory (Figure 10: 1045, 1046).

Ansari et al. and Kisliakov do not explicitly teach a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key. Kocher et al., in an analogous art, however a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key (Figure 2: 265). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Ansari et al. to include a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key. This modification would have been obvious because a person having ordinary skill in the art would have been motivated by the desire to improve the security of systems used to distribute and protect digital content as suggested by Kocher et al. in (Column 5: lines 55-60).

As per claim 4:

Ansari et al. disclose an apparatus, wherein the core logic further comprises a descrambler shared by the first CA logic block and the second CA logic block to descramble the incoming data (Page 2: 0021).

As per claim 5:

Kocher et al. disclose an apparatus, wherein each of the first CA logic block and the second CA logic block further comprises a descrambler to descramble the incoming data (Figure 2: 260).

As per claim 6:

Kocher et al. disclose an apparatus, wherein the core logic further comprises a metal shield surrounding the processor core, the secure non-volatile memory and the non-volatile memory, the shield being made of a conductive material over which power is supplied to the secure non-volatile memory (Kocher et al. suggests making expensive for physically invasive attack (Column 6: lines 50-64).

As per claim 7:

Kisliakov teaches an apparatus, wherein the key is erased from the secure non-volatile memory if a supply of power is disrupted to the secure non-volatile memory due to tampering of the shield (Figure 10: 1053).

As per claim 8:

Ansari et al. disclose an apparatus, wherein the first and second CA logic blocks are one-time programmable logic devices (Figure 1: 50).

As per claim 9:

Kocher et al. disclose an apparatus, wherein the first and second CA logic blocks are field programmable gate arrays (Column 16: lines 1-5).

As per claim 10:

Ansari et al. disclose an apparatus, wherein the first CA function differs from the second CA function (Page 2: 0018, 0021, 0023; Figure 1: 50, 52, 54, 62).

As per claim 14:

Kocher et al. disclose an apparatus, wherein each of the plurality of conditional access logic blocks is a field programmable gate array (Column 16: lines 1-5).

As per claim 15:

Ansari et al. disclose an apparatus, wherein each of the plurality of conditional access logic blocks is a one-time programmable logic device (Figure 1: 50).

As per claim 16:

Kisliakov teaches an apparatus, wherein each of the plurality of conditional access logic blocks is battery-backed so that disruption of power will cause all of the plurality of conditional access logic blocks to become inoperative (Figure 10: 1053).

As per claim 17:

Kocher et al. disclose an apparatus, wherein each of the plurality of conditional access logic blocks is a programmable logic device including programmable gates that are programmed at every power-up (Column 25: lines 59-67).

As per claim 18:

Kocher et al. disclose an apparatus, wherein the core logic comprises:

a battery-backed, non-volatile memory to contain a descrambling key (Column 25: lines 59-67; Column 26: lines 5-24); and

a descrambler coupled to the battery-backed non-volatile memory, the descrambler using the descrambling key to program the programmable gates of each of the plurality of conditional access logic blocks (Column 25: lines 59-67; Column 26: lines 5-24).

As per claim 19:

Kisliakov teaches an apparatus, being a network card connected to a set-top box (Figure 8: 817, 813).

As per claim 21:

Kisliakov teaches an apparatus, wherein the programmable gates of the programmable logic device are one-time programmable and battery-backed so that disruption of power will cause the programmable logic device to become inoperative (Figure 10: 1053).

As per claim 22:

Kisliakov teaches an apparatus, wherein the core logic comprising:

a processor core (Figure 10: 1044);

a non-volatile memory accessible by the processor core, the non-volatile memory to contain information in a scrambled format, the information being recovered using the key contained in the secure non-volatile memory (Figure 10: 1045, 1046).

Ansari et al. and Kisliakov do not explicitly teach a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key. Kocher et al., in an analogous art, however a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key (Figure 2: 265) and a shield adapted to cover the processor core, the secure non-volatile memory and the non-volatile memory, the shield being made of a conductive material over which power is supplied to the secure non-volatile memory (Column 21: lines 5-20). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Ansari et al. to include a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key and a shield adapted to cover the processor core, the secure non-volatile memory and the non-volatile memory, the shield being made of a conductive material over which power is supplied to the secure non-volatile

memory. This modification would have been obvious because a person having ordinary skill in the art would have been motivated by the desire to improve the security of systems used to distribute and protect digital content as suggested by Kocher et al. in (Column 5: lines 55-60).

As per claim 23:

Kocher et al. disclose an apparatus, wherein the programmable gates of the programmable logic device are programmed at every power-up (Column 25: lines 59-67).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See the notice of reference cited in form PTO-892 for additional prior art

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Techane J. Gergiso whose telephone number is (571) 272-3784 and fax number is **(571) 273-3784**. The examiner can normally be reached on 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T-6

Techane Gergiso

Patent Examiner

Art Unit 2137

April 18, 2006

Emmanuel L. Moise
EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER